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EXAMINER	
BRADLEY, MATTHEW A	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 03/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/771,465	KANAI, HIROKI	
	Examiner	Art Unit	
	Matthew Bradley	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action has been issued in response to amendment filed 6 January 2006. Applicant's arguments have been carefully and fully considered in light of the instant amendment, but are moot in view of the new ground(s) of rejection. Accordingly, this action has been made FINAL.

Claims Status

Original claims 1-14 remain pending and are ready for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Takamoto et al (U.S. 5,640,596) hereinafter referred to as Takamoto.

As per independent claim **1**, Takamoto teach,

- a channel controller for receiving a data input/output request based on file-name indication from an information processing device through a network and transmitting/receiving data to/from the information processing device; (Figure 1 item 108) *The Examiner notes that the figure is described in Column 4 line 35 to Column 5 line 14.*

- a disk controller for carrying out input/output control of data stored in a storage volume for storing the data; (Figure 1 item 131) *The Examiner notes that the figure is described in Column 4 line 35 to Column 5 line 14.*
- a first memory for storing the data delivered between the channel controller and the disk controller; and (Figure 1 item 138) *The Examiner notes that the figure is described in Column 4 line 35 to Column 5 line 14.*
- a data transfer network connected to said channel controller, said disk controller and said first memory, (Figure 1 item 142) *The Examiner notes that the figure is described in Column 4 line 35 to Column 5 line 14. The channel control paths are taught in Column 5 lines 30-31.*
- wherein the channel controller is equipped with a first processor for outputting a block-basis I/O request corresponding to the data input/output request and controlling the first memory, (Figure 1 item 136). *The Examiner notes that as the requests are input/output requests to a disk storage device that t he requests will be filled as blocks. Accordingly, the I/O requests are block-basis requests.*
- a file access circuit which has a second processor and a second memory controlled by the second processor and serves to control the transmission/reception of the data input/output request and the data sent from the information processing device (Figure 1 items 137 and 139 as taught in Column 4 line 35 to Column 5 line 14),

- a data transfer device for controlling data transfer between the first memory and the second memory, (Figure 1) *The Examiner notes that the control processors of Figure 1 are all interconnected via communication paths. Accordingly, the communication paths interconnections to the control processors allow for data transfer and as such are data transfer devices.*
- and a third memory controlled by the first processor, (Figure 1 item 141)
- which are formed on a circuit module, and, *The Examiner notes that as file servers are being taught by Takamoto, it is inherent that the individual server components are formed on a circuit module.*
- wherein the second processor transmits information indicating the storage position of the data in the second memory to the first processor, (Column 9 lines 43-54)
- the first processor writes into the third memory data transfer information containing information indicating the storage position of the data in the first memory and information indicating the storage position of the data in the second memory, (Column 11 lines 26-44)
- and the data transfer device reads out the data transfer information from the third memory and controls the data transfer between the first memory and the second memory on the basis of the data transfer information thus read out. (Column 12 lines 28-41).

As per independent claim **2**, Takamoto teach,

- *The Examiner notes that independent claim 2 adds the following limitation to independent claim 1:*
  - transmits the storage position of the data transfer information in the third memory to the data transfer device, (Column 11 lines 26-44)
- *The remaining limitations of claim 2 are rejected on the same grounds of rejection as independent claim 1.*

As per independent claim **3**, Takamoto teach,

- *The Examiner notes that independent claim 3 adds the following limitation to independent claim 1:*
  - wherein the first processor writes into the third memory first data transfer information containing information indicating the storage position of the data in the first memory, (Column 12 lines 28-41)
  - the second processor writes into the second memory second data transfer information containing information indicating the storage position of the data in the second memory, (Column 12 lines 28-41)
  - and the data transfer device reads out the second data transfer information from the second memory, reads out the first data transfer information from the third memory, and controls the data transfer between the first memory and the second memory on the basis of the first data transfer information and the second data transfer information.

The remaining limitations of claim 3 are rejected on the same grounds of rejection as independent claim 1.

As per independent claim **4**, Takamoto teach,

- *The Examiner notes that independent claim 4 adds the following limitation to independent claim 1:*
  - and wherein the first processor writes into the third memory first data transfer information containing information indicating the storage position of the data in the first memory, the second processor writes into the second memory second data transfer information containing information indicating the storage position of the data in the second memory, (Column 12 lines 13-27)
  - the second processor transmits information indicating the storage position of the second data transfer information to the first processor, the first processor transmits to the data transfer device transfer start information containing information indicating the storage position of the first data transfer information and information indicating the storage position of the second data transfer information, (Column 12 lines 13-27)
  - and the data transfer device reads out the second data transfer information from the second memory on the basis of the transfer start information, reads out the first data transfer from the third memory on the basis of the transfer start information, and controls the data transfer between the first memory and the second memory on the basis of the

first data transfer information and the second data transfer information (Column 12 lines 13-27).

The remaining limitations of claim 4 are rejected on the same grounds of rejection as independent claim 1.

As per dependent claim **5**, Takamoto teach, wherein the data transfer device writes into the third memory information indicating the result of the data transfer carried out between the first memory and the second memory (Column 12 lines 31-36).

As per independent claim **6**, Takamoto teach,

- a channel controller for receiving a data writing request based on a file-name indication and writing data from an information processing device through a network; (Figure 1 item 108)
- a disk controller for writing the writing data into a storage volume in which data are stored; (Figure 1 item 131)
- a first memory for storing the writing data transmitted/received between the channel controller and the disk controller; and (Figure 1 item 138)
- a data transfer network connected to said channel controller, said disk controller and said first memory (Figure 1 item 142)
- wherein the channel controller contains a first processor for outputting a block-basis write request corresponding to the data writing request and controlling the first memory, (Figure 1 item 136)
- a file access circuit which has a second processor and a second memory controlled by the second processor and serves to receive the data writing request

and the writing data from the information processing device, (Figure 1 items 137 and 138 as taught in Column 4 line 35 to Column 5 line 14)

- a data transfer device for controlling the data transfer between the first memory and the second memory, (Figure 1) *The Examiner notes that the control processors of Figure 1 are all interconnected via communication paths. Accordingly, the communication paths interconnections to the control processors allow for data transfer and as such are data transfer devices.*
- and a third memory controlled by the first processor, (Figure 1 item 141)
- which are formed on a circuit board, and *The Examiner notes that as file servers are being taught by Takamoto, it is inherent that the individual server components are formed on a circuit board.*
- wherein the first processor writes into the third memory first data transfer information containing information indicating the storage position of the writing data in the first memory, the second processor writes into the second memory second data transfer information containing information indicating the storage position of the writing data in the second memory and transmits information indicating the storage position of the second data transfer information to the first processor, (Column 12 lines 13-36)
- the first processor transmits the data transfer device transfer start information containing information indicating the storage position of the first data transfer information and information indicating the storage position of the second data transfer information, the data transfer device reads out the second data transfer

information from the second memory on the basis of the transfer start information, reads out the first data transfer information from the third memory on the basis of the transfer start information and transfers the writing data from the second memory to the first memory on the basis of the first data transfer information and the second data transfer information, (Column 12 lines 13-41)

- and the disk controller writes into the storage volume the writing data stored in the first memory on the basis of the write request (Column 12 lines 40-41).

As per independent claim **7**, Takamoto teach,

- a channel controller for receiving a data read- out request based on a file-name indication from an information processing device through a network and transmitting to the information processing device read-out data read out from a storage volume for storing data; (Figure 1 item 108)
- a disk controller for reading out the read-out data from the storage volume; (Figure 1 item 131)
- a first memory for storing the read-out data transmitted/ received for the storage volume between the channel controller and the disk controller; and (Figure 1 item 138)
- a data transfer network connected to said channel controller, said disk controller and said first memory (Figure 1 item 142)
- wherein the channel controller comprises a first processor for outputting a block-basis read request corresponding to the data read-out request and controlling the first memory, (Figure 1 item 136)

- a file access circuit which has a second processor and a second memory for controlling the second processor and receives the data read-out request from the information processing device, (Figure 1 items 137 and 139 as taught in Column 4 line 35 to Column 5 line 14)
- a data transfer device for controlling the data transfer between the first memory and the second memory, and (Figure 1)
- a third memory controlled by the first memory, (Figure 1 item 141)
- which are formed on a circuit board, *The Examiner notes that as file servers are being taught by Takamoto, it is inherent that the individual server components are formed on a circuit board.*
- and wherein the disk controller writes into the first memory the read-out data read out from the storage volume on the basis of the read request, the first processor writes into the third memory first data transfer information containing information indicating the storage position of the read-out data in the first memory, the second processor writes into the second memory second data transfer information containing information indicating the storage position of the read-out data in the second memory and transmits information indicating the storage position of the second data transfer information to the first processor, (Column 12 lines 13-46)
- transmits to the data transfer device transfer start information containing information indicating the storage position of the first data transfer information and information indicating the storage position of the second data transfer

information, the data transfer device reads out the second data transfer information from the second memory based on the transfer start information, reads out the first data transfer information from the third memory on the basis of the transfer start information and transfers the read-out data from the first memory to the second memory on the basis of the first data transfer information and the second data transfer information , and the second processor transmits the read-out data stored in the second memory to the information processing device. (Column 12 lines 13-46).

As per independent claim **8**, independent claim **1** discloses a system for performing the method as disclosed in independent claim **8** and is therefore rejected on the same grounds as independent claim **1**.

As per independent claim **9**, independent claim **2** discloses a system for performing the method as disclosed in independent claim **9** and is therefore rejected on the same grounds as independent claim **2**.

As per independent claim **10**, independent claim **3** discloses a system for performing the method as disclosed in independent claim **10** and is therefore rejected on the same grounds as independent claim **3**.

As per independent claim **11**, independent claim **4** discloses a system for performing the method as disclosed in independent claim **11** and is therefore rejected on the same grounds as independent claim **4**.

As per dependent claim **12**, dependent claim **5** discloses a system for performing the method as disclosed in dependent claim **12** and is therefore rejected on the same grounds as dependent claim **5**.

As per independent claim **13**, independent claim **6** discloses a system for performing the method as disclosed in independent claim **13** and is therefore rejected on the same grounds as independent claim **6**.

As per independent claim **14**, independent claim **7** discloses a system for performing the method as disclosed in independent claim **14** and is therefore rejected on the same grounds as independent claim **7**.

Response to Arguments

Applicant's arguments with respect to claims 1-14 have been carefully and fully considered but are moot in view of the new ground(s) of rejection.

The Examiner notes that the applicant's have not presented arguments with respect to claims 5-14 as shown on page 23 of the instant remarks, "reconsideration and withdrawal of these rejections of claims **1-4** is respectfully requested" (emphasis added). Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Bradley whose telephone number is (571) 272-8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DAS/mb

DONALD SPARKS
SUPERVISORY PATENT EXAMINER